REMARKS/ARGUMENTS

The above amendment has cancelled withdrawn claims 11-20 and has placed dependent claims 8 and 10 in independent form, including the subject matter of intervening dependent claims. Accordingly, the amendment places all of the claims in better condition for allowance or appeal.

Claims 1-2 and 5-6 stand rejected under 35 U.S.C. §102(b) over U.S. Patent No. 5,793,989 (Moss). The rejection as to claim 1 is improper, at least because Moss nowhere teaches: (1) a common set of pins coupled to first and second interface circuits and a host computer bus; (2) such common set of pins communicating with the host computer bus in accordance with either a first or second bus standard; or (3) the common set of pins being user selectable.

As to point (1), the Office Action contends that the common set of pins is taught by Moss as element 105, which Moss teaches is a female mechanical connector. Moss, col. 2, lns. 32-33. However, this connector is not coupled to both multiple interface circuits *and* a host computer bus. In fact, this female connector is not coupled to either of the multiple interface circuits or host computer bus in Moss. In this regard, the Office Action contends that the interface circuits are met by PCMCIA logic 112 and alternate interface logic 113 of Moss, while the recited host computer bus is met by an I/O bus 127. Final Office Action, p. 5. However, female connector 105 is not coupled to any of these elements of Moss, contrary to the Examiner's contention. Instead, Moss teaches that the connector 105 is connected to a card logic unit 111 and a corresponding mechanical connector 107 of an applications device 103. *E.g.*, Moss, Fig. 1. As such, the peripheral device 101 of which connector 105 is a part is not coupled to a host computer bus. Instead, it is simply coupled to the applications device 103. Accordingly, Moss fails to teach a common set of pins coupled to both of multiple interface circuits and a host computer bus.

Furthermore, as to point (2) Moss nowhere teaches that such (non-existent) common pins communicate with the host computer bus in accordance with either of the first or second bus standards. In fact, Moss teaches absolutely the opposite. That is, in Moss only RS-232 signals are communicated with I/O bus 127 (contended by the Examiner to be the computer bus). Moss, col. 2, lns. 29-31. Because claim 1 recites that communication *with a host computer bus* is to be

in accordance with either of two bus standards, the permanent RS-232 connection to I/O bus 127 taught in Moss cannot meet the claimed subject matter.

As to point (3), the Office Action apparently contends that the common set of pins of Moss is user selectable by a mode selecting means (FIG. 2, item 201). However, Moss nowhere teaches that this mode selecting logic 201 is user selectable. Instead Moss teaches that the address selecting switches 204 of logic 201 are used to create a uniquely defined combination of address and/or control line states. Moss, 4:1-5. Rather than teaching user selectability, Moss instead teaches that this unique definition is provided by connection of pins when adapting a peripheral device 101 to the applications device 103. Moss, 4:5-8. Simply put, there is no teaching or suggestion of user selectability. Further, no matter how socket logic unit 109 (which includes mode selecting logic 201) is set, communication with the host computer bus is still only with regard to a single bus standard. Accordingly, the rejection of claim 1 and claims 2 and 5-6 depending therefrom is improper and should be reversed.

Claims 3 and 4 stand rejected under 35 U.S.C. § 103(a) over Moss in view of Tyson "How PCI Works." This rejection is improper at least for the same reasons described above regarding claim 1. Furthermore, while Tyson teaches that computers can use a PCI bus to connect peripherals, there is no suggestion or motivation to combine such a bus with the peripheral device of Moss. In this regard, "the mere fact that references can be combined or modified does not render the resulting combination obvious unless the prior art also suggests the desirability of the combination." *In re Mills,* 16 U.S.P.Q.2d 1430 (Fed. Cir. 1990). As such, the rejection of claims 3 and 4 is improper as neither reference provides any rationale suggesting the desirability of the combination. MPEP §2143.01.

Claim 7-8 stand rejected under 35 U.S.C. §103(a) over Moss. In addition to the reasons discussed above regarding claim 1, the rejection is improper as there is no teaching or suggestion in Moss to somehow modify itself to provide an interface circuit that formats signals on an internal bus that is coupled to both interface circuits. Instead in Moss, dedicated buses exist, namely dedicated buses 114 and 116 and dedicated buses 115 and 119, each of which provides signals of only a single bus standard to the corresponding interface circuit. For the further reason that Moss nowhere teaches a single internal bus that is coupled to multiple interface circuits, the rejection of claims 7 and 8 is further overcome.

Note further with regard to claim 8 that it has been placed in independent form such that claim 8 itself recites, in addition to the first and second interface circuits and common set of pins of claim 1, that the first interface circuit is configured to format signals on the recited internal bus compliant with the first bus standard and the second interface circuit is configured to format signals on the internal bus compliant with the second bus standard.

Claim 9 stands rejected under §103(a) over Moss in view of U.S. Patent No. 6,871,244 (Cahill). The rejection of claim 9 is improper for at least the same reasons discussed above regarding claim 1. Furthermore, there is no motivation or suggestion in either of the references to combine the subject matter of Cahill with that of Moss. Accordingly, the rejection of claim 9 is improper and should be reversed.

Note that with regard to claim 10, it has been rewritten in independent form including the subject matter of intervening dependent claim 9. For the further reason that neither reference anywhere teaches or suggests multiple power supplies each to supply voltage swings in accordance with a different bus standard, claim 10 is further patentable.

In view of these remarks, the application is now in condition for allowance and the Examiner's prompt action in accordance therewith is respectfully requested. The Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account No. 20-1504.

Respectfully submitted,

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